

# SELECTED TOPICS IN ADVANCED ELECTRONICS

Edited by  
Khalid A. S. Al-Khateeb



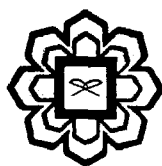
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**ADVANCED ELECTRONICS**

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## **CHAPTER 32**

### **CIRCUIT DESIGN OF A CLOCK DATA RECOVERY**

By

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#### **Synopsis**

This chapter focuses on the design of the clock data recovery (CDR) circuit for the receiver circuit. The design issues related to the CDR circuit are recovered clock jitter and limited frequency/phase acquisition range. The main function of a clock and data recovery (CDR) circuit is to extract a clock from incoming data stream and sample the received data with the extracted clock as illustrated in Fig. 1. CDR circuits generate clocks for input data streams without reference clocks. There are two different forms of basic CDR architectures such as non-self correcting and self-correcting architecture.

#### **3. Introduction**

Aggressive scaling in the CMOS technology has brought numerous advantages in terms of lower power, area reduction and higher speeds of digital integrated circuit systems. These benefits have to be supported by efficient inter-chip communication before it can have a dramatic effect on the overall system (Hanumolu, Wei et al. 2008). In computer systems where numerous hardware devices are connected to the CPU (Central Processing Unit), the speed, reliability and efficiency of the computer bus is a matter of critical importance. As the speed of the microprocessors' have grown exponentially, its system interface data rates and supporting channel have to keep up so that bottlenecks in the system do not occur. The Peripheral Component Interconnect Express (PCIe), is a local bus that handles communications between all the hardware devices and the CPU. The PCIe buses which are capable of handling large bandwidths of data can be represented as Input-output (I/O) links which consist of a transmitter, channel and receiver. Refer to Fig. 1. The PCIe bus can reside in the CPU itself or be implemented as a separate chip. The transmitter sends the data to the